

FIG. 3A

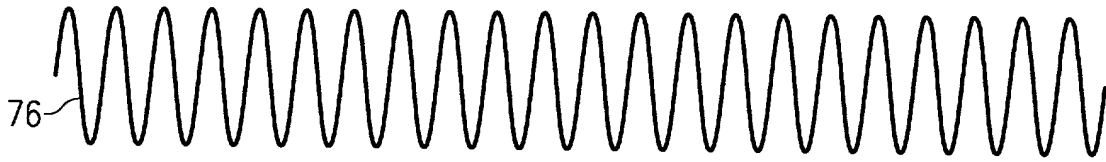


FIG. 3B

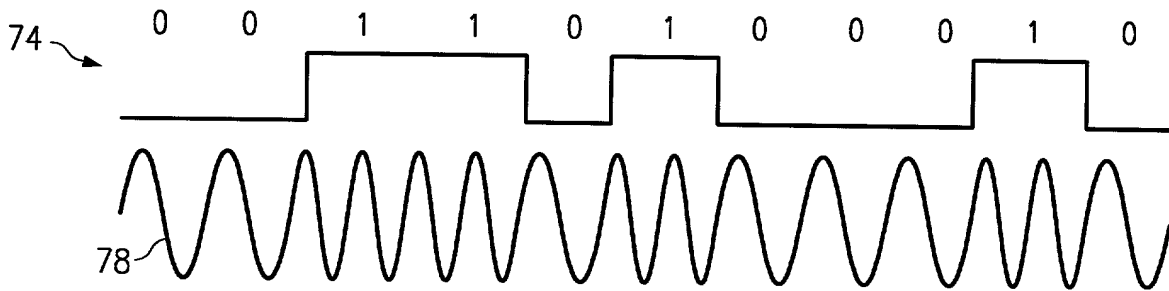


FIG. 3C

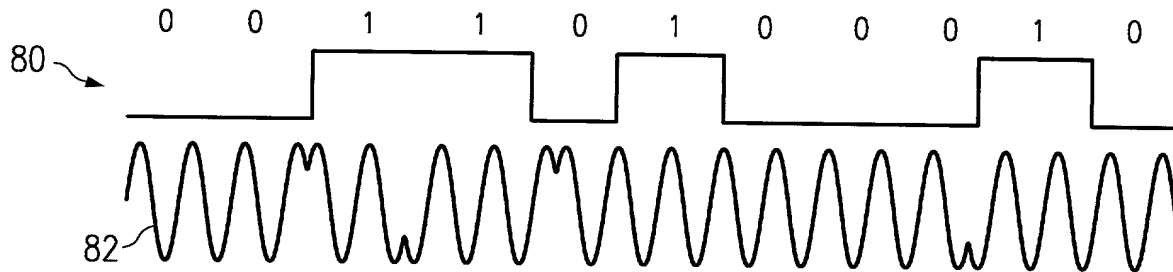
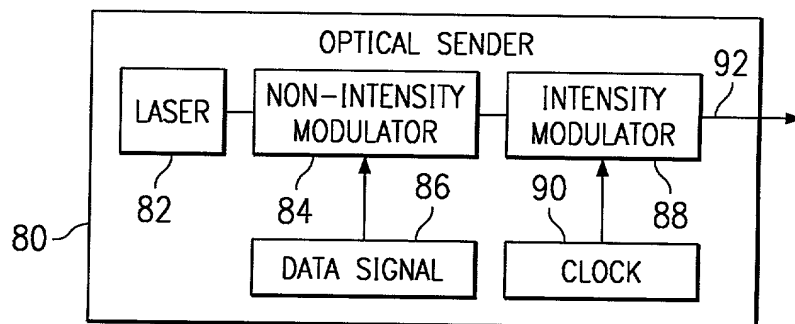


FIG. 4



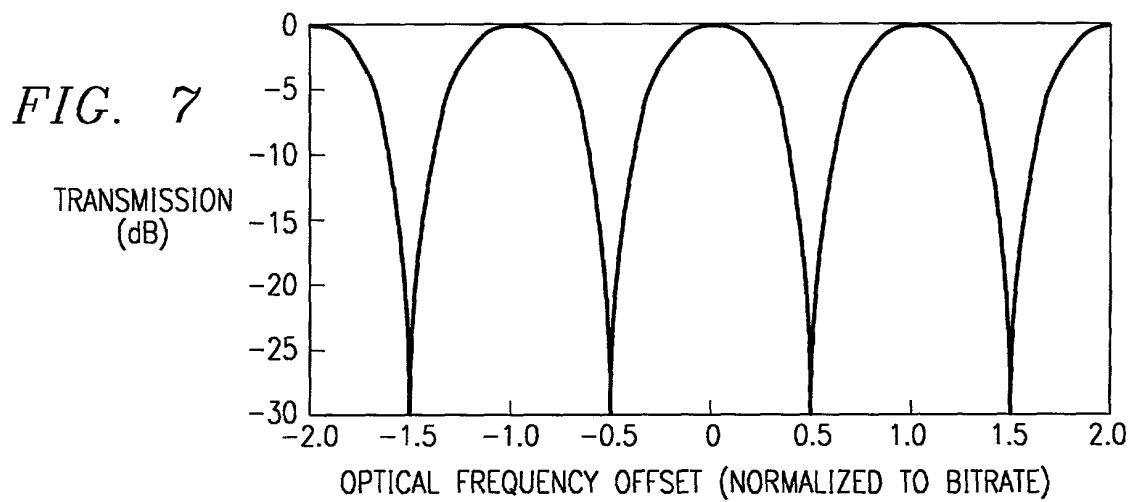
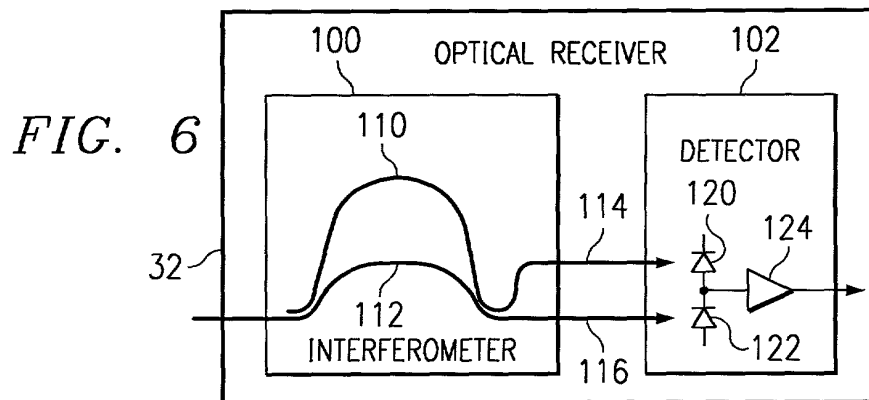
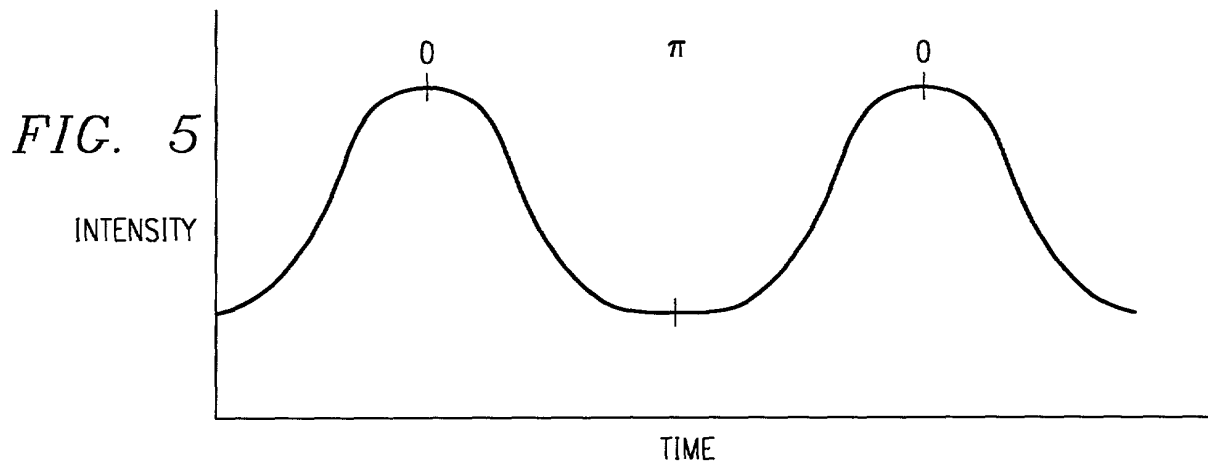


FIG. 8A

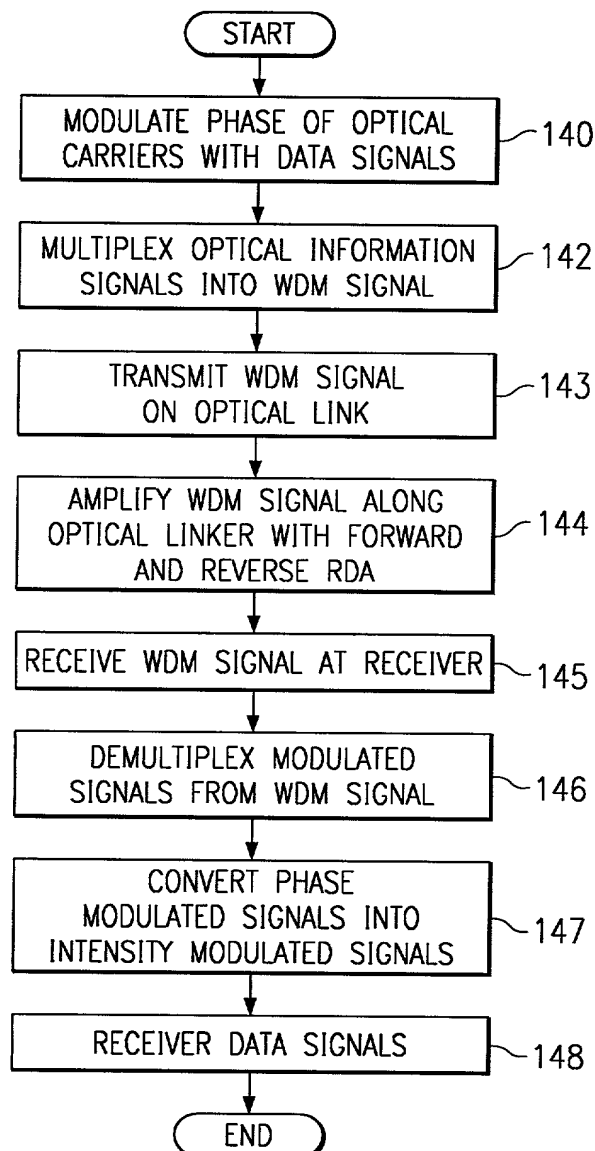
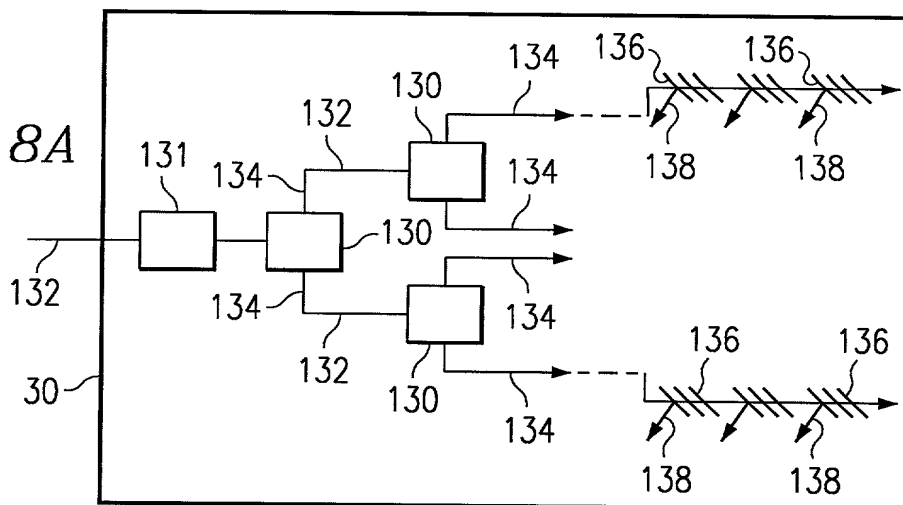


FIG. 9

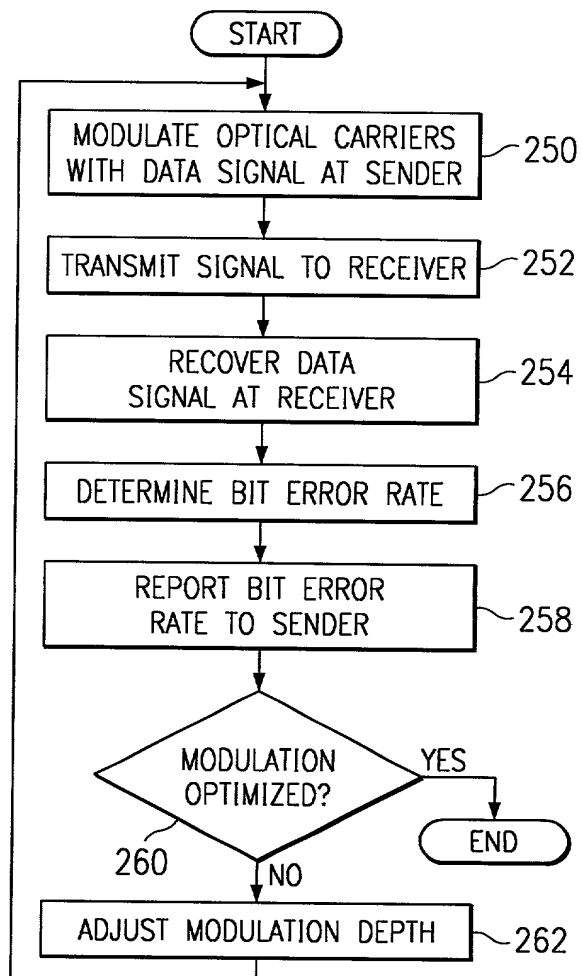


FIG. 13

FIG. 8B

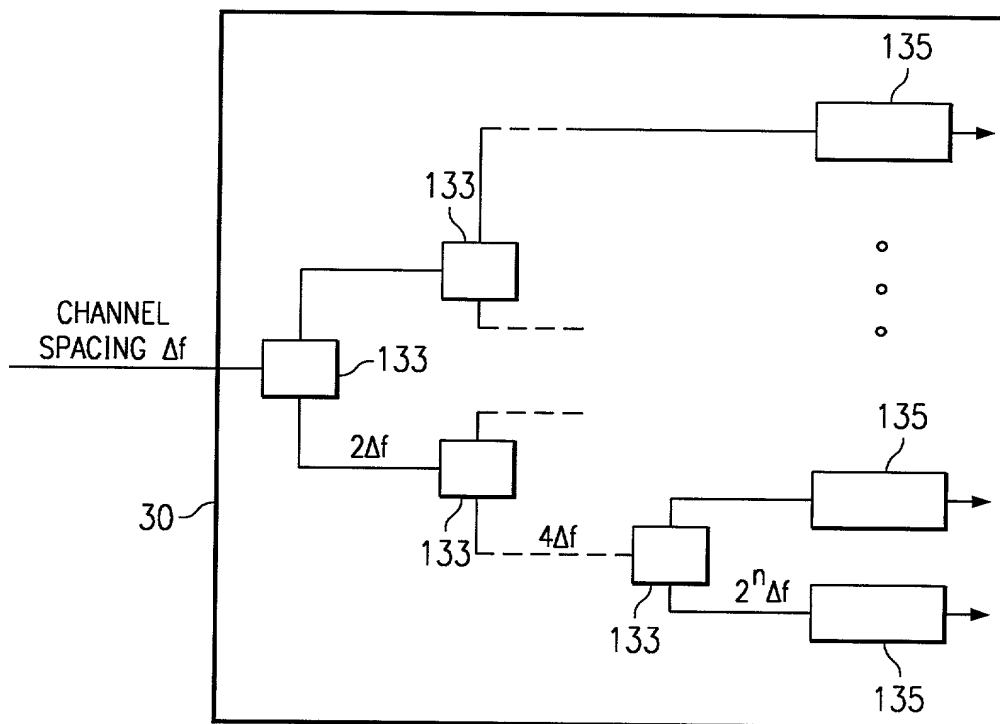
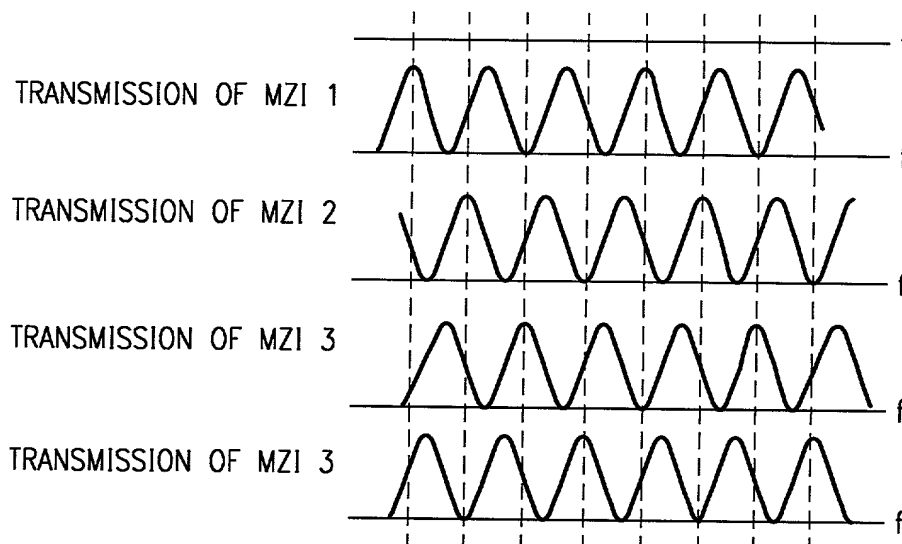


FIG. 8C

WDM CHANNEL ALLOCATION



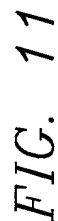
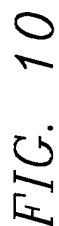


FIG. 12

```
graph LR
    LASER[210] -- 234 --> PM[PHASE MODULATOR]
    subgraph System [ ]
        direction TB
        BC1[BIAS CIRCUIT 230] --> ED1[ELECTRICAL DRIVER 232]
        DS[DATA SIGNAL 214] --> ED1
        ED1 --> PM
        BC2[BIAS CIRCUIT 240] --> ED2[ELECTRICAL DRIVER 242]
        CK[CLOCK 244] --> ED2
        ED2 --> IM[INTENSITY MODULATOR 246]
    end
    PM -- 236 --> IM
    IM -- 248 --> Out[ ]
    CONTROLLER[216] --> BC1
    CONTROLLER --> BC2
    CONTROLLER --> DS
    CONTROLLER --> CK
```

FIG. 14

275

297 290 294 292

296 λ_1 OS 294

λ_{CLK} OS 294

290 \vdots

λ_n OS 294

297 290 294

TRANSMITTER

298

284

282

WDM DEMUX

294

OR 312 λ_1 297

OR 312 λ_{CLK} 297

\vdots 312

OR 312 λ_n 297

RECEIVER

```

graph LR
    320((320)) --- J(( ))
    J --- 322[INTERFEROMETER 322]
    J --- 326[CLOCK RECOVERY 326]
    322 --- 324[DETECTOR 324]
    326 --- 332[332]
    332 --- 324
    326 --- 330[330]
    330 --- 334[DATA RECOVERY 334]
    subgraph 15 [15]
        322
        324
        326
        330
        334
    end
    style 15 fill:none,stroke:none

```